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APPLICATION NO.		FILING DATE		FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
	10/518,736 12/16/2		/2004	Antonius Maria Petru Johannes Hendriks	NL02 0528 US	1311
	65913	7590	05/30/2007		EXAMINER	
		NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE		SCHILLINGER, LAURA M		
				ART UNIT	PAPER NUMBER	
	SAN JOSE, C		<del>-</del> · -		2813	
					MAN DATE	DELIVERY MODE
					MAIL DATE	DELIVERY MODE
				•	05/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)					
. Office Assistant Community	10/518,736	HENDRIKS ET AL.					
Office Action Summary	Examiner	Art Unit					
<u> </u>	Laura M. Schillinger	2813					
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).							
Status							
Responsive to communication(s) filed on 12 Fe     This action is FINAL. 2b) ☑ This     Since this application is in condition for allowant closed in accordance with the practice under E	action is non-final.  ice except for formal matters, pro						
Disposition of Claims							
4)							
Priority under 35 U.S.C. § 119							
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  a) All b) Some * c) None of:  1. Certified copies of the priority documents have been received.  2. Certified copies of the priority documents have been received in Application No  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  * See the attached detailed Office action for a list of the certified copies not received.							
Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date	4)  Interview Summary Paper No(s)/Mail Da 5)  Notice of Informal Pa 6)  Other:	te					

## **DETAILED ACTION**

#### Claim Objections

Claims 3, 5 and 11 are objected to because of the following informalities: Claims 3 and 5 need commas at the end of their respective limitations and claim 11 contains a typo. Appropriate correction is required.

### Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen (129).

Chen teaches the following claimed limitations as cited below:

1. (Previously Presented) Method for manufacturing on a substrate a semiconductor device with a floating-gate and a control-gate, comprising the steps of:

first forming isolation zones in the substrate (Fig. 7 (22)),

thereafter forming a floating gate on the substrate between two isolation zones (Fig. 7 (25)),

thereafter extending the floating gate using conductive spacers (Fig. 7 (24)), and

thereafter forming a control gate over the floating gate and the conductive spacers (Fig.8 (30)).

2. (Previously Presented) Method according to claim 1, wherein the step of forming the floating gate comprises:

providing the floating gate on the substrate, the floating gate having two opposite walls located above the isolation zones (Fig.2 (12)),

forming a recess in the isolation zones under the opposite walls of the floating gate (Fig.2 (21)).

3. (Previously Presented) Method according to claim 2, wherein the step of providing the floating gate, comprises:

depositing a floating gate layer (Fig.2 (12),

forming slits in the floating gate layer, thus forming the opposite walls of the floating gate (Fig.2 (21)).

4. (Original) Method according to claim 2, wherein the step of extending the floating gate comprises

depositing a conductive layer on the opposite walls of the floating gate and on the walls of the recess in the isolation zones (Fig.6 (23)).

5. (Original) Method according to claim 4, wherein the step of depositing a conductive layer on the opposite walls of the floating gate and on the walls of the recesses in the isolation zones comprises depositing a conductive layer over the floating gate and in the recesses in the isolation zones (Fig.6 (23)),

etching the conductive layer (Fig.7).

- 6. (Original) Method according to claim 1, further comprising a step of forming a dielectric layer on the floating gate and on the conductive spacers before forming the control gate.(Fig.8 (26))
- 9. (Original) Method according to claim 2, wherein a recess in an isolation zone is formed by etching (Fig.2 (21)).
- 10. (Original) Method according to claim 1, comprising the step of providing a tunnel oxide between the semiconductor substrate and the floating gate (Fig.1 (11)).
- 11. (Previously Presented) Method according to claim 1, wherein the step of forming the control gate comprises: depositing a control gate layer (Fig.8 (30), and patterning the control gate layer to form the control gate (Col.6, lines: 5-10).
- 12. (Original) Method according to claim 1, wherein the conductive spacers are polysilicon spacers (Col.5, lines 55-56).

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

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having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen ('129).

Chen teaches to isolate the substrate using a FOX region however fails to teach the limitations of claims 7 and 8 as repeated below:

- 7. (Original) Method according to claim 1, wherein the isolation zones are shallow trench isolation (STI) zones.
- 8. (Original) Method according to claim 1, wherein the isolation zones are LOCOS regions.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chen's teachings to use STI or LOCOS as a different means of isolation since such isolation techniques are well known to one of ordinary skill and considered to be conventional substitutions.

#### **Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M. Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

05/21/07

Laura M Schillinger Primary Examiner Art Unit 2813